What is Claimed is:

1. Apparatus for measuring the power consumed by a processing unit processor bus during predetermined period of time, the apparatus comprising:

a central processing unit, the central processing unit including a trace port, the central processing unit executing a program, the central processing unit applying to a trace port trace signals resulting from the execution of the program;

a trace unit for receiving trace information from the trace port;

a first memory unit portion coupled to the trace unit for storing the trace information;

a second memory portion for storing a simulation model of the central processing unit; and

a processor coupled to the first and the second memory portion; the processor determining power consumption for the program execution of the central processing unit.

2. The apparatus as recited in claim 1 wherein the processor uses trace information applied to the simulation model to determine a state of the central processing unit for each central processing unit clock cycle.

3. The apparatus as recited in claim 2 wherein the processor stores parameters identifying the power dissipated for each state of the central processing unit.

4. The apparatus as recited in claim 3 wherein the parameters identifying the power dissipated for each state is determined by simulation techniques.

5. The apparatus as recited in claim 1 wherein the central processing unit and the processor are the same processing component.

6. A method for determining power consumption by a central processing unit during execution of a program, the method comprising:

executing the program by the central processing unit;

acquiring and storing the trace information for the central processing unit for each central processing unit clock cycle;

determining from a simulation model of the central processing unit the power consumption parameter for each state of the central processing unit;

using the trace information generated by the central processing unit and the simulation model to determine the state of the central processing unit as determined by the simulation model; and

using the power consumption parameters, determining the power consumption for the executing program.

7. The method as recited in claim 6 wherein the power consumption is determined for each central processing unit clock cycle.

8. The method as recited in claim 6 wherein the power consumption parameters are determined by simulation techniques.

9. The method as recited in claim 6 wherein the power consumption is correlated with the execution of the program.

10. The method as recited in claim 6 wherein the using steps are performed by the central processing unit.

11. Apparatus for determining the power consumption during activity of a digital signal processing unit, the digital signal processing unit including trace export apparatus, the apparatus comprising:

a trace unit coupled to trace export apparatus in the digital signal processing unit, the trace unit receiving trace information from the digital signal processing unit, the trace unit storing the trace information of the digital signal processing unit;

a first memory unit portion for storing the trace information from the digital signal processing unit;

a second memory unit portion storing a simulation model of the digital signal processing unit; and

a processor coupled to the first memory portion and the second memory portion, the processor determining the state of the of the digital signal processing unit by applying the trace information to the simulation model to identify the state progression of the digital signal processor, the state progression determining the energy consumed by digital signal processing unit.

12. The apparatus as recited in claim 11 wherein the second memory portion stores power consumed for each digital signal processing unit state for each clock cycle.

13. The apparatus as recited in claim 12 wherein the power consumed for each digital signal processing unit state is determined by simulation techniques.

14. The apparatus as recited in claim 11 wherein the trace information are determined for each clock cycle.

15. The apparatus as recited in claim 14 wherein the power consumed by the digital signal processing unit is correlated to the activity.

16. The apparatus as recited in claim 11 wherein the digital signal processing unit is a central processing unit.

17. The apparatus as recited in claim 11 wherein the digital signal processing unit and the processor are the same component.

18. A data processing system for determining the power consumed in response to an activity of a central processing unit, the data processing system comprising:

a central processing unit, the central processing unit including trace export apparatus;

a first storage unit portion coupled to the central processing unit;

a trace unit coupled to the trace export apparatus and the first storage portion, the trace unit storing trace information generated in response to the activity on the central processing unit; and

a second storage unit portion, the second storage unit portion having a simulation model of the central processing unit stored therein, the second storage portion storing values of the energy consumption for each state;

wherein the central processing unit applies the trace information to each the simulation model to determine the state progression of central processing unit states during the activity, the central processing unit using the energy consumption value for each state of the state progression to determine the total power consumed by the central processing unit during the activity.

19. The data processing system as recited in claim 18 wherein the power consumption values are determined by simulation techniques.